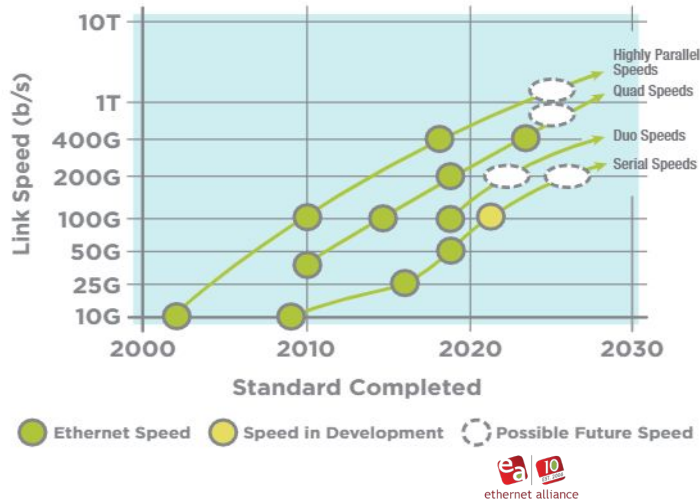


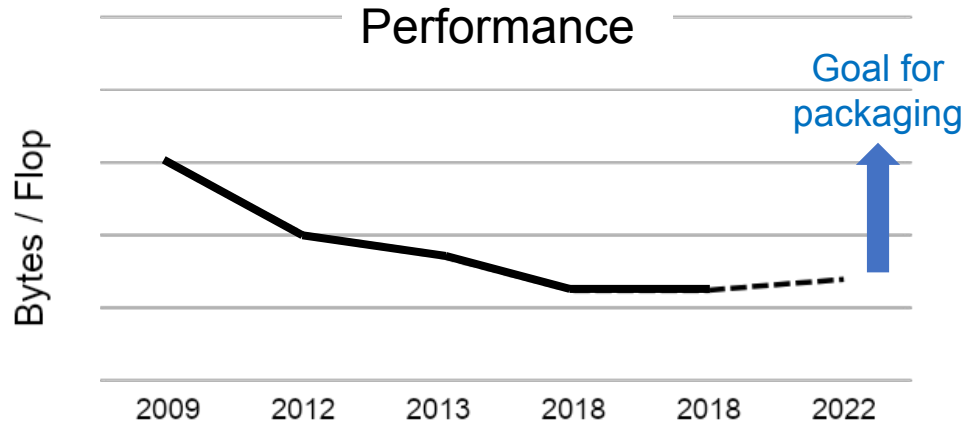
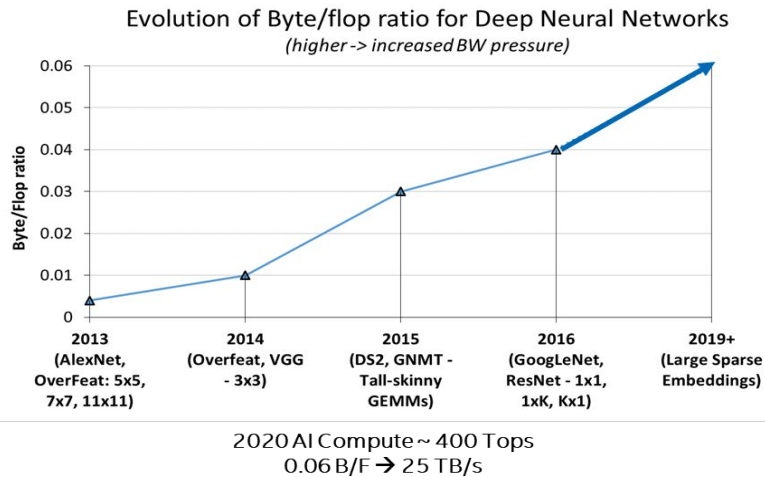
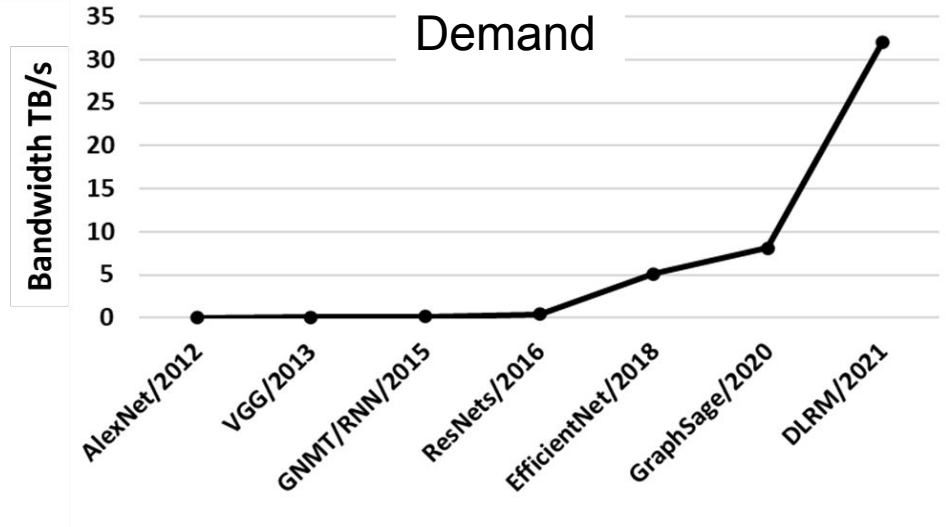


Heterogeneous Integration (HI) Part 2

I/O Bandwidth & Speed Scaling Trends



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*2022 represents trends and not actual data

↑ Growing BW Demand ↑ Dense Interconnects

Interconnect Scaling to Enable Bandwidth Scaling

Peripheral Interconnects for Solder Based 2D Architectures

Generations		1	2	3	4	5
Raw Bandwidth Density (GBps/mm)		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (μm)	55	50	40	35	30
	IO/mm	500	667	1000	1500	2000
	IO/mm ²	331	400	625	816	1111
Signaling Speed	Gbps	2	3	4	5.33	8

Generation Number →		1	2	3	4	5
Raw Linear Bandwidth Density (GBps/mm)		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (μm)	55	40	30	20	10
	Linear Escape Density (IO/mm)	500	667	1000	2000	4000
	Areal Escape Density (IO/mm ²)	331	625	1111	2500	10000
Signaling Speed (Gbps)		2	3	4	4	4

Source : Chapter 22 in IEEE Heterogeneous Integration Roadmap
<https://eps.ieee.org/technology/heterogeneous-integration-roadmap/2021-edition.html>

Interconnect Scaling to Enable Bandwidth Scaling

Area Interconnects for 3D Architectures

Generations		1	2	3	4	5
Raw Bandwidth Density (Gbps/mm ²)		125	250	500	1000	2000
Package Technology	Minimum Bump Pitch (μm)	40	30	20	15	10
	IO/mm ²	625	1111	2500	4444	10000
Signaling Speed	Gbps	1.6	1.8	1.6	1.8	1.6

Key Metrics

Key Metrics and Adoption Criteria

Key Performance Indicators

- Bandwidth density (linear & area)
 - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
 - Scalable energy consumption
 - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+Rx)
- Channel Reach
 - Technology, frequency, & BER
- Reliability & Availability
- Cost
 - Standard vs advanced packaging

UCIe - Architected and specified from the ground-up to deliver the best KPIs while meeting wide adoption criteria

Factors Affecting Wide Adoption

- Interoperability
 - Full-stack, plug-and-play with existing s/w is+
 - Different usages/segments
- Technology
 - Across process nodes & packaging options
 - Power delivery & cooling
 - Repair strategy (failure/yield improvement)
 - Debug – controllability & observability
- Broad industry support / Open ecosystem
 - Learnings from other standards efforts



UCIe 1.0 delivers the best KPIs while meeting the projected needs for the next 5-6 years. Wide industry leader adoption spanning semiconductor, manufacturing, assembly, & cloud segments.

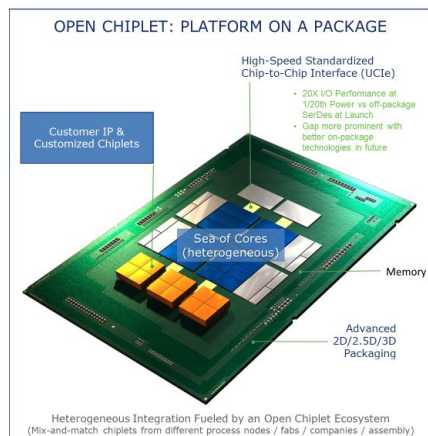


UCIe 1.0: Characteristics and Key Metrics

CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 – 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<= 2	

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm²)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5ns <= 16G, 0.5-1ns >= 24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) < 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode

Motivation



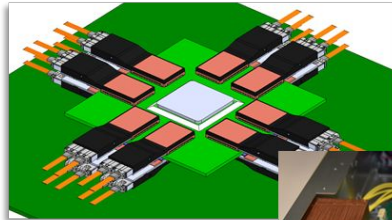
Align Industry around an open platform to enable chiplet based solutions

- Enables construction of SoCs that exceed maximum reticle size
 - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
 - Enables optimal process technologies
 - Smaller (better yield)
 - Reduces IP porting costs
 - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing and process locked IPs)



Mainstreaming Optical Interconnects

Intel Demonstrates Industry-First Co-Packaged Optics Ethernet Switch



Designed for

- Total BW 12.8 Tbps
- 8 optical engines @ 1.6 Tbps each
- 16 0.1Tbps channels for each engine



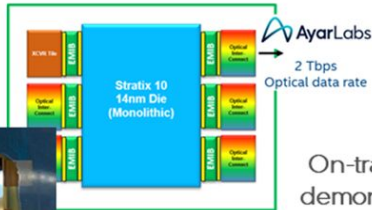
Ref:

<https://newsroom.intel.com/news/intel-demonstrates-industry-first-co-packaged-optics-ethernet-switch/#gs.l2pnld>

	Copper (PCIe 6)	OIO	Cu vs. OIO
Shoreline density (bi-directional)	380 Gb/s/mm	800 Gb/s/mm → 1.6 Tb/s/mm	4x
Reach	12"	>100m	>100x
Latency	<10ns	<10ns	Similar for short reach
Power efficiency	Opportunity for 35% reduction		
Per-wire pair/ per-fiber bandwidth	64Gb/s	512Gb/s → 1Tb/s	8-16x

Demonstrated integration of 1 OIO tile via EmIB/ AIB on DARPA CHIPS

REF: <https://www.darpa.mil/news-events/2020-02-25>



On-track to demonstrate multiple OIO tiles in PIPES program



Co-Packaged optics complements Cu signaling and enables new topologies
cost, technology maturity and high yield manufacturing are key challenges

Ref: "Co-Packaged Photonics For High Performance Computing: Status, Challenges And Opportunities," in Journal of Lightwave Technology, vol. 40, no. 2, 2022

Summary



- Scaling 2D and 3D Die-to-Die interconnects will ensure continued bandwidth scaling
- “Plug and Play” through D2D link standardization will ensure systematic growth
- Co-Packaging Optics is a key element of future off-package bandwidth scaling

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